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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/751,610
Filing Date: December 29, 2000
Appellant(s): HARRIS, WILLIAM A.

Robert E. Mates
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/9/2006 appealing from the Office action mailed 4/28/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

Li	USP 5,058,132	10/1991
Epstein	USP 4,093,870	6/1978

MANO " Computer Engineering Hardware Design", pages 130-132, 1988.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 20-24, 26-29, 31-37, 39-45 and 47-48 are rejected under 35USC 103(a) as being unpatentable over Li (USP 5,058,132) in view of Epstein (USP 4,093,870) and Mano (Computer Engineering Hardware Design, 1988, pages 130-132).

Figure 2 of Li shows a circuit for dividing an input clock signal into N clock signals having a relative phase separating of 360/2N, where N (N is 5, column 5, lines 50-64) is a positive integer, the circuit comprising: a phase locked loop (102) receiving an input signal (116) having a frequency F0 (125 Mhz) and providing an output signal ((signal 124 having a signal of 2NF0 = 12.5 Mhz) having a frequency of 2NF0, a Johnson counter (114) having N stages (5 flip flops, column 5, lines 50-64) connected to receive as an input the output signal (124) of the phase locked loop circuit (102) and providing an output signal (LBC1-5) as an error signal to the phase locked loop circuit (column 5, lines 25-28), and the Johnson counter (114) having at least 5 flip flop circuits (stages), also connected for providing at least two output signals (LBC1-5)

from at least two of the N stages of the Johnson counter (114) as clock signals each having a phase displaced from the phase of the other 360/2N degrees.

Li reference does not disclose the Johnson counter (114) having N JK flip flops with the particular arrangement as called for in claims 1, 20, 32 and 40. Epstein's figure 4 discloses a Johnson counter using JK flip flops with a particular arrangement as claimed. Mano's reference further teaches that JK flip flop is reliable because it does not have the undermined states (page 131, third paragraph). Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to implement the 5 stages (flip flop circuits) Johnson counter of Li with a five JK flip flop circuit arranged as in Epstein because JK flip flop is reliable thus preventing the counter from erroneous operation.

Regarding claims 2-3, 21, 33-34, 41-42 and 48, the combination of Li, Epstein and Mano references discloses N is 5. However, depending on the frequency of the input signal, the output frequency of the VCO can be divided up or down (N =4 required in claims 2, 21, 33 and 41; N =8 required in claims 3, 34, 42 and 48) to be in synchronized with the input signal without changing the overall operation of the circuit. Thus, the dividend factor N is a design expedient dependent on the particular application. Therefore, the limitation of using N equals 4 or 8 as recited in claims 2, 21 and 3 will not be patentable under 35USC 103(a).

Regarding claim 22, each signal LBC1-5 has a frequency of 2NF0.

Regarding claims 23 and 35-36, the error signal (output of the VCO of Li) has a frequency equal to F0.

Regarding claims 24, 29, 37 and 45, Li shows a phase detection (104), low pass filter and gain stage (106) and VCO (108).

Regarding claims 26, 31, 39 and 47, each Q output and complementary Q output of each JK flip flop is coupled to provide a clock signal, the 2N clock signals having relative phase separation of 360/2N degree, and each clock signal having a frequency F0.

Regarding claims 27 and 43-44, the feedback signal is seen as the feedback in (123) of Li reference.

Regarding claim 28, each clock output has a frequency F0.

(10) Response to Argument

Appellant's arguments filed 01/09/2006 have been fully considered but they are not persuasive.

Appellant argues the combination of Li (USP 5,058,132), Epstein (USP 4,093,870) and Mano references fails show evidence of reasonable expectation of success is not persuasive. Epstein's figure 4 discloses a Johnson counter using JK flip flops with a particular arrangement as claimed. Mano's reference further teaches that JK flip flop is reliable because it does not have the undermined states (page 131, third paragraph). Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to implement Li's Johnson counter with JK flip flop circuits arranged as in Epstein because JK flip flop is reliable thus preventing the counter from erroneous operation. Thus, the combination provides an evidence of a reasonable expectation of success, i.e., an error free JK Johnson counter.

Appellant argues that the combination of Li (USP 5,058,132), Epstein (USP 4,093,870) and Mano references does not show a Johnson counter comprising an input JK flip flop, an output JK flip flop, and a plurality of middle JK flip flops as called for in the independent claims 1, 20, 32 and 40 is not persuasive. As noted above under the 35USC 103(a) section, Li

reference suggests that the Johnson counter (114) is a divide by ten (column 5, lines 55). This suggests a plurality of stages Johnson counter. Epstein's figure 4 discloses a divide by six Johnson counter (each flip flop is a divide by two and Epstein shows three JK flip flop circuits). Therefore, to form a divide by ten, five JK flip flop circuits are needed. Therefore, it would have been obvious to implement Li's Johnson counter with five JK flip flop circuits arranged as in Epstein because JK flip flop is reliable thus preventing the counter from erroneous operation.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

2/16/2006

Conferees:

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